PATENT ABSTRACTS OF JAPAN

(11)Publication number : **06-061810**
(43)Date of publication of application : **04.03.1994**

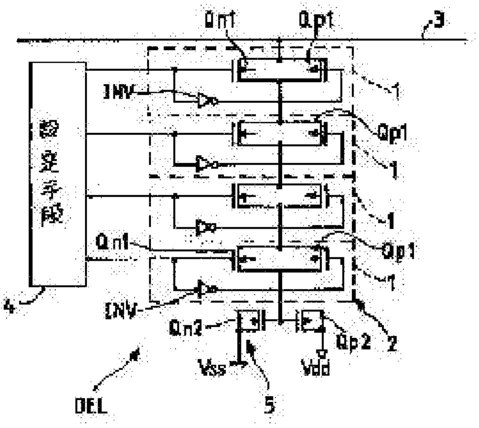
(51)Int.Cl. H03K 5/135
G06F 1/10
H01L 27/04

(21)Application number : **04-236552**
(22)Date of filing : **12.08.1992**

(71)Applicant : **HITACHI LTD**
(72)Inventor : **KAWAI SHINTARO**
YAMAGISHI MIKIO
MASUDA NOBORU

(54) VARIABLE DELAY CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING IT

(57)Abstract:
PURPOSE: To adjust the phase of a clock signal while the number of components and power consumption are reduced by adopting not a gate load but a CMOS transfer gate for the production of a delay.
CONSTITUTION: CMOS transmission gates 1 are controlled sequentially to be in the ON state from the gate 1 at a clock signal line side. Then a gate-source capacitance, a gate-drain capacitance and a diode capacitance of the gates to be turned on are added sequentially to the clock signal line 3, and the result is equivalent to the increase in the capacitive component as a delay component of the signal line 3. As a result, the linearity with a very small variable width is obtained for the control performance of a delay time with respect to a clock signal propagated through the signal line 3. Furthermore, no through-current flows to a variable capacitor means 2 and the capacitive component obtained by one MOS TR is larger than that of a gate load. Thus, the phase adjustment for the clock signal is implemented with a comparatively smaller number of components than that of the gate load while suppressing the increase in the power consumption.



* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]One side of a capacity electrode between a capacity electrode of another side of a capacitative element and a clock signal line which were combined with a power supply, A variable delay circuit being what forms a setting-out means to determine capacity value which has a variable-capacity means to provide two or more complementary MOS transfer gates which carried out the series connection, set up a switch state of said complementary MOS transfer gate, and was seen from said clock signal line side.
[Claim 2]The variable delay circuit according to claim 1 which is provided with the following and characterized by a gate of both MOS transistors being what constitutes a capacity electrode of said another side.
N channel type MOS transistor by which sauce and a drain are combined with earth potentials as for said capacitative element.
P channel type MOS transistor by which sauce and a drain are combined with power supply potential.

[Claim 3]The variable delay circuit according to claim 1 or 2 which combines two or more said variable-capacity means with said clock signal line in parallel, and is characterized by each variable-capacity means being what is controlled by said setting-out means.
[Claim 4]A circuit which combined two or more said variable-capacity means in parallel is further combined with said clock signal line via a selector gate, The variable delay circuit according to claim 3, wherein a variable-capacity means combined with a clock signal line without passing a variable-capacity means and a selector gate which are combined with a clock signal line via a selector gate is what is controlled by a signal generated by said setting-out means in common.
[Claim 5]Said same variable-capacity means is mutually combined with an input side and an output side of a circuit element which were inserted in said clock signal line in same number [every] plurality parallel, The variable delay circuit according to claim 1 or 2, wherein a variable-capacity means combined with an output side of a variable-capacity means combined with an input side of a circuit element and said circuit element is what is controlled by a signal generated by said setting-out means in common.
[Claim 6]To an input side and an output side of a circuit element which were inserted in said clock signal line, further, A circuit which combined said same variable-capacity means in same number [every] plurality parallel is mutually combined via a selector gate, A variable-capacity means combined with a clock signal line without passing a variable-capacity means and a selector gate which are combined with a clock signal line via a selector gate in both sides of an input side of said circuit element and an output side, The variable delay circuit according to claim 5 being what controlled by a signal generated by said setting-out means in common.
[Claim 7]A clock pulse generator and a frequency divider which carries out dividing of the clock signal generated by this, A semiconductor integrated circuit device being what is formed in one semiconductor substrate including a variable delay circuit of claim 1 thru/or 6 connected to a signal wire of a clock signal acquired in a frequency divider given in any 1 paragraph, and changes.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention about art to the clock adjustment of a variable delay circuit, and the phase / frequency separation (PF separation) control system further for high-speed LSI applied to the phase adjustment of a clock signal, For example, it applies to the circuitry which requires the double-izing mechanism of minute variable and variable width to a clock signal phase, and is related with effective art.
[0002]
[Description of the Prior Art]The conventional variable delay circuit is roughly classified into two. The thing of the P/F separation method with which one used gate load, and another are the PLL (phase locked loop) circuits using VCO (voltage controlled oscillator). When using gate load, various gates are arranged at a clock course. In using a PLL circuit, it carries out by inserting a circuit suitable between a phase comparator and VOC, and multiplying frequency. As an example of the literature in which the circuitry of such frequency multiplying was indicated, there is the 65th page of ″integrated circuit application handbook″ of Asakura Publishing Issue on June 30, Showa 56.
[0003]
[Problem(s) to be Solved by the Invention]However, in the delay circuit of the P/F separation method using gate load, the amount of gates to be used becomes large and increase of an element number and power consumption is caused. There is no lineality in the controllability of a time delay, and phase adjustment of a clock signal cannot be easily performed by minute variable width. It was shown clearly that it was hard to realize the variable delay circuit of the PLL system using VCO in CMOS.
[0004]There is the purpose of this invention in providing the variable delay circuit which can perform phase adjustment of a clock signal, suppressing increase of power consumption by a comparatively small element number compared with gate load. Another purpose of this invention is to provide the variable delay circuit which has linearity in the controllability of the time delay over a clock signal (phase adjustment is possible by minute variable width). Another purpose of this invention is to provide a variable delay circuit realizable in a CMOS circuit in addition to the purpose of each above.
[0005]The other purposes and the new feature will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0006]
[Means for Solving the Problem]It will be as follows if an outline of a typical thing is briefly explained among inventions indicated in this application.
[0007]Namely, two or more complementary MOS transfer gates which carried out the series connection are adopted as a variable-capacity means, This is connected to a clock signal line, a setting-out means to determine capacity value which set up a switch state of said complementary MOS transfer gate, and was seen from said node is formed, and a variable delay circuit is constituted.
[0008]What is necessary is to combine two or more variable-capacity means with a clock signal line in parallel, and just to carry out switch control of the complementary MOS transfer gate of a variable-capacity means separately, in order to enlarge variable width of delay as a whole.
[0009]In order to make inclination of delay change selectable, to said clock signal signal wire further, What is necessary is just to control in common a variable-capacity means combined with a clock signal line without passing a variable-capacity means and a selector gate which combine a circuit which combined two or more said variable-capacity means in parallel via a selector gate, and are combined with a clock signal line via a selector gate by a signal generated by a setting-out means.
[0010]In order to take correspondence between an input side of a circuit element and an output side which were inserted in said clock signal line and to set up delay, a circuit which comprises said variable-capacity

means is made equal by the input side and output side, and both circuits are controlled by said setting-out means in common.

[0011]

[Function]If the complementary MOS transfer gate is controlled from the signal wire side to an ON state one by one according to the above-mentioned means, It is proportional to the number of the complementary MOS transfer gates made into the ON state, The capacity between gate drains and diode capacity are added to a signal wire one by one between the gate sauce of the complementary MOS transfer gate, It becomes equivalent to the capacity component as a delay ingredient of a signal wire having increased, and this gives linearity to the controllability of the time delay over the clock signal spread to a signal wire by minute variable width. The capacity component which a variable-capacity means does not send penetration current, and is obtained by one MOS transistor in a variable-capacity means is comparatively large compared with gate load, This realizes the variable delay circuit which can perform phase adjustment of a clock signal, suppressing increase of power consumption by a comparatively small element number compared with gate load.

[0012]

[Example]One example of the basic form of variable delay circuit DEL concerning this invention is shown in drawing 1. The basic form of a variable delay circuit is provided with the plurality 1, for example, four complementary MOS (it is only described also as CMOS below) transfer gates, which carried out the series connection as the variable-capacity means 2, This is connected to the clock signal line 3, and a means (it is described also as a setting-out means below) 4 to determine the capacity value which set up the switch state of said complementary MOS transfer gate 1, and was seen from said node is formed, and it is constituted. Each CMOS transfer gate 1 connects P channel type MOS transistor Qp1 and N channel type MOS transistor Qn1 in parallel via a source drain, The signal by which level reversal was carried out is mutually supplied to transistor Qp1 of both sides, and Qn1 gate via the inverter INV. N channel type MOS transistor Qn2 by which sauce and a drain are combined with the termination of this variable-capacity means 2 by the earth potentials Vss, Sauce and a drain are provided with P channel type MOS transistor Qp2 combined with the power supply potential Vdd, and the capacitative element 5 from which it is combined with the termination of the variable-capacity means 2 and which the gate of MOS transistorQn2 of both sides and Qp2 comprises is arranged.

[0013]Switch control of each CMOS transfer gate 1 is carried out by the output of said setting-out means 4. For example, when the setting-out means 4 is provided with the flip-flop which carries out a one to one correspondence to the CMOS transfer gate 1, according to the state of the flip-flop, switch control of the CMOS transfer gate 1 is carried out. It can initialize by CPU (central processing unit) or a data processing means like a microprocessor, or especially the state of a flip-flop can be controlled according to the decoded result of the signal for several bits given by passing an external terminal etc., although not restricted. What is necessary is just to relate the combination of the signal level for several of the bits with clock signal frequency, in determining a delaying amount according to the frequency of the clock signal spread to the clock signal line 3.

[0014]If the CMOS transfer gate 1 is controlled from the clock signal line 3 side to an ON state one by one, It is proportional to the number of the CMOS transfer gates 1 made into the ON state, The capacity between gate drains and diode capacity are added to the clock signal line 3 one by one between the gate sauce of the CMOS transfer gate 1, and it twists equivalent to the capacity component as a delay ingredient of the clock signal line 3 having increased. The linearity which had minute variable width in the controllability of the time delay over the clock signal spread to the clock signal line 3 by this can be obtained. In [the capacity component of the variable-capacity means 2 which does not send penetration current and is obtained by one MOS transistor is comparatively large compared with gate load, and] this point, Phase adjustment of a clock signal can be performed suppressing increase of power consumption by a comparatively small element number compared with gate load.

[0015]Various examples which applied the basic form of drawing 1 are shown in drawing 2. In drawing 2, said capacitative element 5 has omitted the graphic display. The capacitative element 5 may be exclusive-use-ized for each variable-capacity means 2, or may be shared by two or more variable-capacity means 2.

[0016]In (A) of drawing 2, the inverter 6 is inserted in the clock signal line as a circuit element. It functions on this inverter 6 as waveform shaping or the clock driver of a clock signal. At this time, the one variable-capacity means 2 is arranged to each input side and output side of the inverter 6, respectively, and both variable-capacity means 2 are controlled by said one setting-out means 4 in common. That is, the setting-out means 4 outputs the switch control signal S1 - S4, for example, the switch control signal S1 carries out switch control of the CMOS transfer gate 1 by the side of the top in the variable-capacity means of both the input side of the inverter 6, and an output side in common. Thereby, correspondence can be taken between the input side of the inverter 6, and an output side, and delay can be set up.

[0017]In (B) of drawing 2, the variable-capacity means 2 for four rows is arranged in parallel to each of the input side of the inverter 6, and an output side, and the variable-capacity means 2 is controlled by the input side and an output side by said setting-out means 4 in common to it at said the appearance. In this case, the setting-out means 4 outputs the switch control signals S1-S16. Thereby, compared with the case of (A) of drawing 2, variable width of delay can be enlarged as a whole. This situation is clear if (B) is compared with (A) of drawing 3. (A) of drawing 3 corresponds to drawing 2 (A), and (B) of drawing 3 is a characteristic figure corresponding to (B) of drawing 2. In drawing 3, a vertical axis expresses a time delay (ns), and a horizontal axis expresses the number of the CMOS transfer gates of an ON state.

[0018]In (C) of drawing 2, further the circuit which combined the variable-capacity means 2 for four rows in parallel via the selector gate 7 to the composition of (B) of drawing 2, It combines with each of the input side of said inverter 6, and an output side, and the connectionless variable-capacity means 2 is controlled by common switch control signal Si (i= 1-16) to the variable-capacity means 2 and the selector gate 7 which were connected to the selector gate 7. This situation is illustrated considering the switch control signal S16 as a representative. Thereby, inclination of delay change can be chosen now by whether the selector gate 7 is made into an ON state, or an OFF state is used. This is clear also from the characteristic figure shown in (C) of drawing 3 corresponding to (C) of drawing 2.

[0019]The one example block diagram of the microcomputer system which applied the variable delay circuit concerning this invention is shown in drawing 4. Although this system in particular is not restricted, A microprocessing unit. (MPU) DRAM made into the workspace of 10, ROM(read only memory) 11 which hold the operation program of the microprocessing unit 10, and microprocessing unit 10 **, or the temporary storage of data. (Dynamic random access memory) DRAM controller 13 for performing refreshment control of 12 and DRAM12, etc., SCI(serial communication interface controller) 14, DMAC. (Direct memory access controller) It has 15, the timer counter 16, etc., and they are connected by bus 17. The various operation clock signals of this system The clock pulse generator 20, It is formed with the frequency divider 21 which carries out dividing of the clock signal generated by this, and the variable delay circuit unit 22 which establishes said variable delay circuit in the signal wire of the clock signal acquired in the frequency divider 21. The clock signal outputted from a variable delay circuit unit is supplied to a necessary circuit module. The microcomputer system shown in drawing 4 may be constituted by the board as the circuit board, and may be constituted as an integrated circuit by one semiconductor substrate like silicon. When integrated-circuit-ized, a bus interface circuit can be built in.

[0020]The details of the clock signal product of drawing 4 are shown in drawing 5. The variable delay circuit unit 22 of drawing 5 is provided with i+1 variable delay circuit DEL0 - DELi. The proper circuitry each variable delay circuit DEL0 - DELi are indicated to be to drawing 1 and drawing 2 is adopted. The time delay set up by variable delay circuit DEL0 - DELi here shall be determined according to the clock signal frequency outputted from the clock pulse generator 20. Supposing selectable clock frequency is eight kinds at this time, in order to show it from the exterior, the signals D0-D2 of a triplet will be given to the logic circuit 23. The logic circuit 23 outputs data required in order to make the CMOS transfer gate 1 of a prescribed number into an ON state to each variable delay circuit DEL0 - DELi corresponding to the directed clock frequency to the setting-out means of a variable delay circuit. For example, the delay control to the clock signal at this time can be made to participate in setting out of the non overlap interval time in 2 phase clock signal of non overlap. Said signals D0-D2 may be any of the signal supplied via an external terminal, or the signal in which initial setting is carried out by the microprocessing unit 10.

[0021]Although the invention made by this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which this invention is not limited to it and does not deviate from the gist. For example, a variable delay circuit can also be arranged in the proper position of a clock signal feed route. The in-series number of stages of the CMOS transfer gate which constitutes a variable-capacity means, and also the parallel number of stages of a variable-capacity means are not limited to the above-mentioned example, but can be changed suitably. The capacitative element located in the termination of a variable-capacity means may not necessarily be CMOS structure. This invention is also applicable as a clock module with composition as shown in drawing 5.

[0022]This invention is applicable to the thing of conditions which needs to adjust the phase of a clock signal at least.

[0023]

[Effect of the Invention]It will be as follows if the effect acquired by the typical thing among the inventions indicated in this application is explained briefly.

[0024](1) Since not gate load but a CMOS transfer gate is used for generating delay, phase adjustment of a clock signal can be performed, suppressing increase of power consumption by a comparatively small element number compared with gate load.
(2) Since a time delay has the number of CMOS transfer gates, and a linear relation, the time delay or phase of a clock signal can be linearly controlled by minute variable width, and it becomes easy to do the phase adjustment of a clock signal, and its design.
(3) Variable width of delay can be enlarged as a whole by combining two or more variable-capacity means with a clock signal line in parallel, and carrying out switch control of the CMOS transfer gate of a variable-capacity means separately.
(4) The circuit which combined two or more variable-capacity means in parallel is further combined with a clock signal line via a selector gate, Inclination of delay change can be chosen now by controlling in common the variable-capacity means combined with a clock signal line without passing the variable-capacity means and selector gate which are combined with a clock signal line via a selector gate by the signal generated by a setting-out means.
(5) By constituting equally the circuit constituted from said variable-capacity means by the input side and output side of the circuit element inserted in the clock signal line, and controlling both circuits by said setting-out means in common, Correspondence can be taken between the input side of a circuit element and output side which were inserted in the clock signal line, and delay can be set up.

[Translation done.]